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Semiconductor Implementation of Differential Correlation and Noncoherent Integration

Andreas Schmid
Infineon Technologies AG Germany
Phone: +49 203 7298 254, Email: Andreas.Schmid@infineon.com

ABSTRACT

Emergency caller location and location based services increasingly lead to navigation receivers being integrated into cellular telephones. The size constraints of cellular phones require highly integrated semiconductor solutions. The cost of microchips can be reduced by shrinking the silicon area. This can be accomplished by the optimum choice of the quantization resolutions in the digital baseband section and by the reuse of hardware resources within the integrated circuits. Since satellite navigation receivers for indoor applications are usually designed to host the equivalent of several thousand correlation channels, the benefit of reducing the bit sizes and reusing the signal processing blocks is substantial. The required amount of signal processing units can be reduced by operating the hardware resources with an increased clock rate and multiplexing different signal processing paths through the same hardware. The implementation of the differential correlation and the noncoherent integration methods in hardware description language allows the synthesizing of the signal processing units into a complementary metal-oxide semiconductor (CMOS) technology. This paper presents the resulting silicon area, power consumption, quantization loss, and timing characteristics. The quantization characteristics are chosen such that the resulting degradation is sufficiently low for enhanced sensitivity Galileo/GPS receivers. The timing slack of the CMOS synthesis results are analyzed in order to estimate the degree of parallelization required for single shot positioning. When compared with the desired sample rates, the timing slack indicates how many correlation channels can be served in parallel by the respective unit.

KEYWORDS: Quantization, Timing, CMOS, Area, Power Consumption.

1. INTRODUCTION

The vast majority of future mobile telephones are expected to be equipped with a satellite navigation receiver. Legislative requirements such as E-911 and E-112 as well as the prospected revenues with location based services have already started to drive the demand for GPS receivers. The majority of future Galileo receivers are also expected to become integrated into mobile phones. Since modern mobile phones support a wide range applications, the satellite navigation receiver needs to be a highly integrated semiconductor solution. The most important requirement for the successful integration of a Galileo/GPS receiver into mobile phones is low cost. The manufacturing costs have a strong impact on the product price. As the microchip becomes smaller, a larger number of them fit on a single wafer and the product price drops. The size can be reduced by the optimum choice of the quantization resolutions in the digital baseband section and by the reuse of hardware resources within the integrated circuits.

2. SEMICONDUCTOR SYNTHESIS

Since modern GPS receiver chips contain from several tens of thousands to several hundreds of thousands of correlation channels, the careful design of the correlation channels is of utmost importance in order to reduce the bit sizes in the correlation channels and to reuse the hardware resources for multiple channels in parallel (Schmid *et al.* 2005), (Schmid 2007). The optimum quantization resolutions for the differential correlation technique, as well as for the state-of-the-art noncoherent integration method are therefore derived in this paper. Furthermore, the required amount of signal processing units can be also substantially reduced. This is accomplished by operating the hardware resources with an increased clock rate and multiplexing different signal processing paths through the same hardware.

The actual silicon area, power consumption, quantization loss, and timing characteristics can only be determined after synthesizing the signal processing units into a semiconductor process. For this paper, the basic operational block for differential correlation and noncoherent integration have been synthesized to an advanced complementary metal-oxide semiconductor (CMOS) process. In order to obtain these results, the respective floating point algorithms are first converted into a fixed point representation and then implemented with the Verilog hardware description language. The units are verified with the Mentor Graphics ModelSim before they are synthesized into digital CMOS circuits with the Synopsys Design Compiler. This tool allows the analysis of the circuit timing characteristics and the silicon area.

Based on the synthesis results, the power consumption of the silicon circuits is simulated with the Sequence Power Theater. The simulations begin with low clock frequencies and extend up to extremely high clock frequencies, as long as the timing slack remains positive. The inputs of all units are directly connected to the processing logic and the output signals are stored in flip-flops. This allows the different units to operate asynchronously from each other, where the signal requires one clock period to propagate through each processing block.

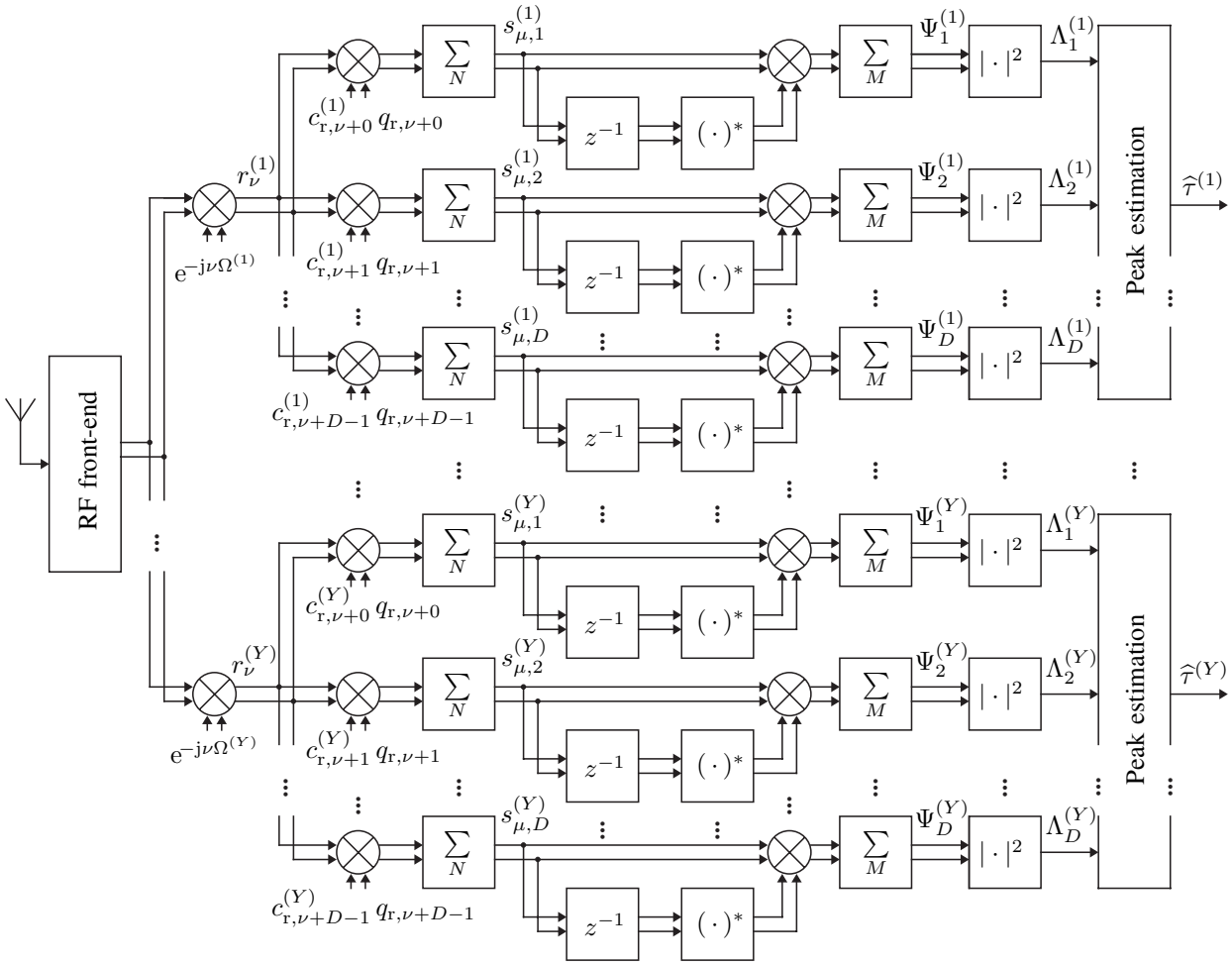
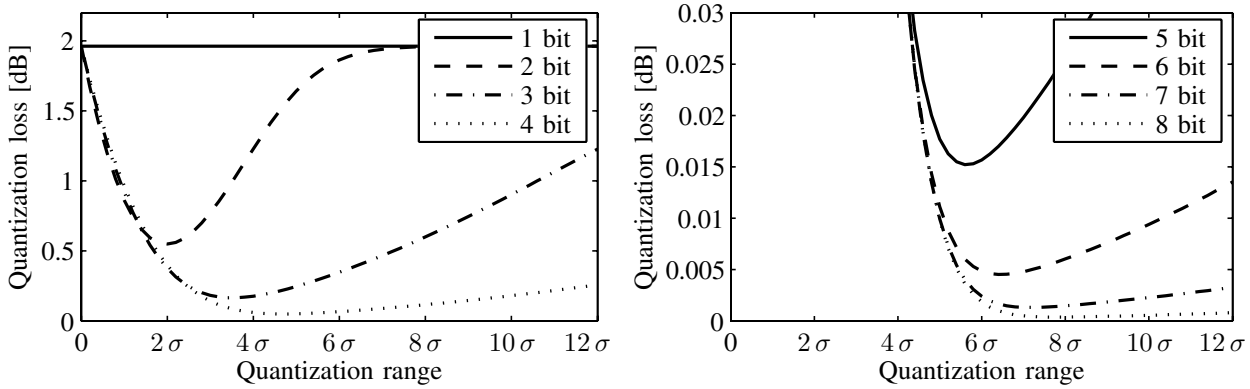


Figure 1. Highly parallel reception with the differential correlation technique.

3. ANALOG TO DIGITAL CONVERSION

Figure 1 provides an overview of the highly parallel differential correlation technique (Schmid and Neubauer 2005), (Schmid 2007). The choice of the quantization resolution for the Analog-to-Digital Conversion (ADC) is determined by the trade-off between the implementation complexity and Signal-to-Noise Ratio (SNR) degradation (Schmid *et al.* 2005), (Schmid 2007). High quantization resolutions offer lower SNR degradation, but introduce substantial implementation expenses. This is because they each require a consecutive digital signal processing stage to operate with correspondingly larger bit ranges. Figure 2 shows the quantization loss for a uniform ADC with a mid-riser characteristic as a function of the number of output bits. The quantization range is given as a multiple of the input standard deviation σ. The optimal quantization range for signals with very low SNR depends almost entirely on the standard deviation of the input signal, which is denoted by σ in Figure 2 (Benvenuto and Cherubini 2002), (Proakis 2001).

Table 1 summarizes the optimum quantization range and the resulting implementation degradation for a given number of output bits (Jeruchim 2000). The output quantization resolution specifies how many bits are used to decode the output signal, the quantization range specifies which range is covered before the saturation takes place and the quantization loss specifies the resulting SNR degradation.



(a) 1–4 bit resolution.

(b) 5–8 bit resolution.

Figure 2. Quantization loss for a uniform ADC with mid-riser characteristic.

Output quantization resolution	Optimal quantization range	Minimal quantization loss
1 bit	n/a	1.96 dB
2 bit	[-0.99 σ, 0.99 σ]	0.55 dB
3 bit	[-1.76 σ, 1.76 σ]	0.17 dB
4 bit	[-2.35 σ, 2.35 σ]	0.050 dB
5 bit	[-2.82 σ, 2.82 σ]	0.015 dB
6 bit	[-3.23 σ, 3.23 σ]	0.0045 dB
7 bit	[-3.58 σ, 3.58 σ]	0.0013 dB
8 bit	[-3.93 σ, 3.93 σ]	0.00038 dB

Table 1. Quantization characteristics for the ADC unit.

Silicon area	Timing slack	Leakage power	Dynamic power
51.7 μm^2	$T_\mathrm{s} - 0.175\,\mathrm{ns}$	30.1 nW	$\frac{9.49 \times 10^{-14}\,\mathrm{W}}{T_\mathrm{s}}$

Table 2. Synthesis results for the despreading unit.

4. DESPREADING

The despreading stage does not cause any implementation loss, as it only multiplies the input signal with a series of ± 1. If the signal encoding is chosen symmetrically around zero with a single bit marking the sign and the remaining bits the magnitude, then the despreading stage only has to perform an exclusive-or (XOR) operation between the input signal bit and the despreading code. Table 2 shows the total silicon area, power consumption and timing slack for different clock frequencies of the despreading unit. The results show that a single despreading unit could, in principle, support the entire search of all code delays. The received signal would be applied at the input and the entire reference code would be stepped through within one chip period of the received signal. During the next chip period of the received signal, the reference code would

Silicon area	Timing slack	Leakage power	Dynamic power
$458\,\mu\mathrm{m}^2$	$T_\mathrm{s} - 0.585\,\mathrm{ns}$	244 nW	$\frac{5.31 \times 10^{-13}\,\mathrm{W}}{T_\mathrm{s}}$

Table 3. Synthesis results for the GOLD code generation unit.

	Accumulation number	Output quantization resolution	Output quantization range	Theoretical quantization loss	Simulated quantization loss
GPS L1-C/A	2045	6 bit	[-2047, 2047]	0.063 dB	0.060 dB
GPS L1-C/A	40900	6 bit	[-4095, 4095]	0.013 dB	0.014 dB
Galileo E1-C	8180	6 bit	[-4095, 4095]	0.063 dB	0.063 dB
Galileo E1-C	40900	6 bit	[-4095, 4095]	0.013 dB	0.016 dB

Table 4. Quantization characteristics for the coherent accumulation unit.

Silicon area	Timing slack	Leakage power	Dynamic power
$760\,\mu\mathrm{m}^2$	$T_\mathrm{s} - 2.89\,\mathrm{ns}$	485 nW	$\frac{1.06 \times 10^{-12}\,\mathrm{W}}{T_\mathrm{s}}$

Table 5. Synthesis results for the coherent accumulation unit.

start with a shift of one chip and again step through the entire code. The reference code generator would thus have to run through the entire code plus one chip within the period of one chip of the received signal. Table 3 presents the implementation characteristics of the GPS L1-C/A GOLD code generator for different clock frequencies. It shows that the code generator could, in principle, also support this multiplexing scheme where the despreading and code generation unit are reused for the despreading with all code delays.

5. COHERENT ACCUMULATION

The coherent accumulation stage integrates N samples of the input signal. The output requires a higher quantization resolution than the input, as the signal-to-noise ratio is also higher at the output. Furthermore, due to the increased mean and standard deviation at the output, a quantization step size larger than one is required. Table 4 summarizes the quantization characteristics and the resulting loss for the coherent accumulation. Table 5 presents the results of the semiconductor synthesis of the coherent accumulation unit.

	Output quantization resolution	Output quantization range	Theoretical quantization loss	Simulated quantization loss
GPS L1-C/A	8 bit	[-1023, 1023]	0.010 dB	0.010 dB
GPS L1-C/A	8 bit	[-1023, 1023]	0.008 dB	0.008 dB
Galileo E1-C	8 bit	[-1023, 1023]	0.005 dB	0.005 dB
Galileo E1-C	8 bit	[-1023, 1023]	0.010 dB	0.011 dB

Table 6. Quantization characteristics for the differential product unit.

Silicon area	Timing slack	Leakage power	Dynamic power
$4839\,\mu\mathrm{m}^2$	$T_\mathrm{s} - 3.73\,\mathrm{ns}$	$3.13\,\mu\mathrm{W}$	$\frac{3.35 \times 10^{-12}\,\mathrm{W}}{T_\mathrm{s}}$

Table 7. Synthesis results for the differential product unit.

	Accumulation number	Output quantization resolution	Output quantization range	Theoretical quantization loss	Simulated quantization loss
GPS L1-C/A	100	8 bit	[-511, 511]	0.001 dB	0.002 dB
Galileo E1-C	100	8 bit	[-511, 511]	0.002 dB	0.002 dB

Table 8. Quantization characteristics for the differential accumulation unit.

6. DIFFERENTIAL PRODUCT

The differential product unit multiplies each input sample with the complex-conjugate of the previous input sample. The complex-valued differential product is implemented with three multiplications, one addition and two subtractions. In order to reduce the silicon area, the three multiplication operations are calculated by a single multiplier in time multiplex operation. Table 6 summarizes the quantization results for the differential product while Table 7 presents the synthesis results.

7. DIFFERENTIAL ACCUMULATION

The differential products are further accumulated to form the differential correlation result. Since the differential correlation result is then processed in software, the output resolution of the differential accumulation stage is 8 bit, which results in an additional quantization loss of just around 0.002 dB. The quantization characteristics of the differential accumulation unit are summarized in Table 8, while the synthesis results are presented in Table 9.

Silicon area	Timing slack	Leakage power	Dynamic power
$895\,\mu\mathrm{m}^2$	$T_\mathrm{s} - 2.06\,\mathrm{ns}$	530 nW	$\frac{9.82 \times 10^{-13}\,\mathrm{W}}{T_\mathrm{s}}$

Table 9. Synthesis results for the differential accumulation unit.

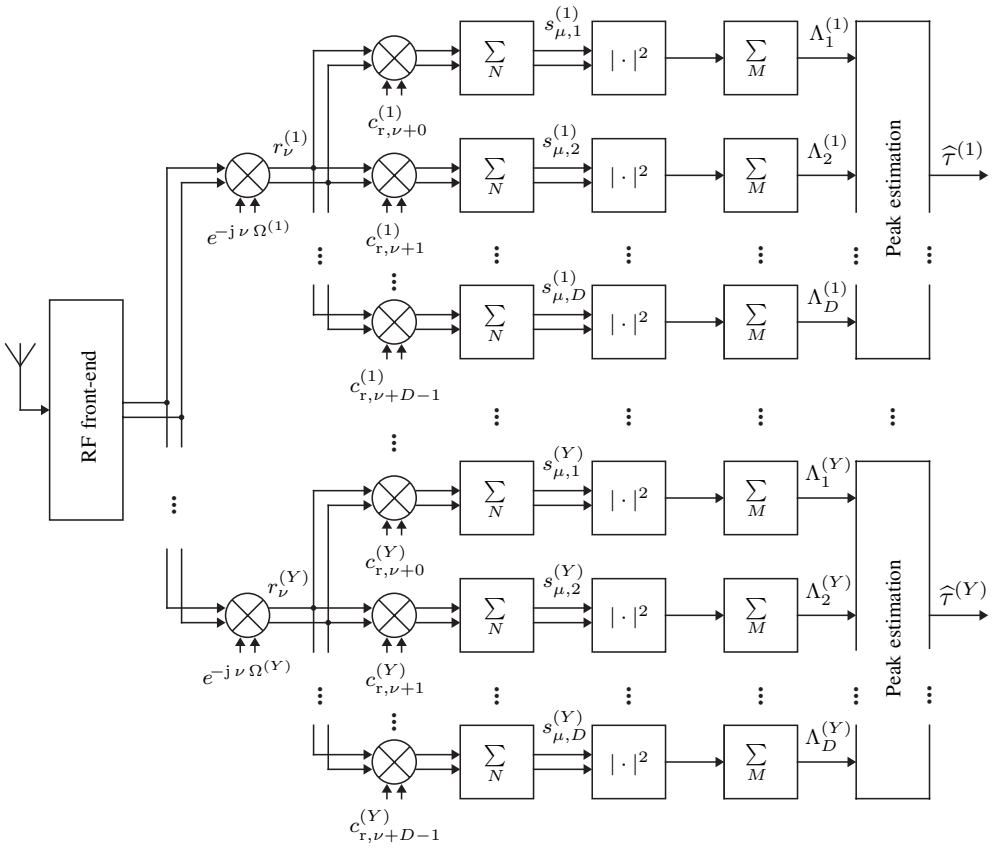


Figure 3. Highly parallel correlation technique with the noncoherent integration method.

8. SQUARED MAGNITUDE

Figure 3 shows an overview of the highly parallel correlation technique with noncoherent integration. The differential correlation technique and the noncoherent integration method use the same signal processing chain up to the coherently integrated predetection results.

For the noncoherent integration method, the inphase and quadrature components of the input are squared and added together by the squared magnitude stage. The internal squaring hardware is thereby reused for both squaring operations in time multiplex mode. Table 10 shows the quantization results and Table 11 summarizes the CMOS semiconductor synthesis outcome.

9. NONCOHERENT ACCUMULATION

The final step for the noncoherent integration method is to raise the signal-to-noise ratio of the detection statistic by means of noncoherent accumulation. This accumulator hardware only

	Output quantization resolution	Output quantization range	Theoretical quantization loss	Simulated quantization loss
GPS L1-C/A	7 bit	[0, 1023]	0.005 dB	0.004 dB
GPS L1-C/A	7 bit	[0, 1023]	0.004 dB	0.012 dB
Galileo E1-C	7 bit	[0, 1023]	0.002 dB	0.001 dB
Galileo E1-C	7 bit	[0, 1023]	0.005 dB	0.014 dB

Table 10. Quantization characteristics for the squared magnitude unit.

Silicon area	Timing slack	Leakage power	Dynamic power
$876\,\mu\mathrm{m}^2$	$T_\mathrm{s} - 1.84\,\mathrm{ns}$	555 nW	$\frac{1.3 \times 10^{-12}\,\mathrm{W}}{T_\mathrm{s}}$

Table 11. Synthesis results for the squared magnitude unit.

	Accumulation number	Output quantization resolution	Output quantization range	Theoretical quantization loss	Simulated quantization loss
GPS L1-C/A	100	8 bit	[0, 2047]	0.003 dB	0.003 dB
Galileo E1-C	100	8 bit	[0, 2047]	0.003 dB	0.003 dB

Table 12. Quantization characteristics for the noncoherent accumulation unit.

Silicon area	Timing slack	Leakage power	Dynamic power
$721\,\mu\mathrm{m}^2$	$T_\mathrm{s} - 2\,\mathrm{ns}$	416 nW	$\frac{8.73 \times 10^{-13}\,\mathrm{W}}{T_\mathrm{s}}$

Table 13. Synthesis results for the noncoherent accumulation unit.

has to process positive numbers, since its input is supplied by the squared magnitude unit. It can hence be implemented with less silicon area than the differential accumulation unit. The silicon area is displayed in Table 13 together with the timing and power characteristics, while the quantization loss is found in Table 12.

10. CONCLUSION

This paper presents the semiconductor implementation characteristics for differential correlation and noncoherent integration. The quantization resolutions are a trade-off between maximizing the signal-to-noise ratio and minimizing the silicon area. The resulting quantization degradation is sufficiently low for enhanced sensitivity Galileo/GPS receivers. A large number of correlation results can be calculated simultaneously by running the hardware units with an increased clock rate and multiplexing the data streams. The timing slack of the CMOS synthesis can be analyzed

in order to estimate the degree of parallelization required for single shot positioning. When compared with the desired sample rates, the timing slack indicates how many parallel correlation channels can be served by the respective unit. The simulations of the power consumption allow an estimate of the battery drain by the receiver circuit. The silicon area does not increase with the clock frequency as long as the timing slack is positive. Combined with the required degree of parallelization, the synthesized silicon area is important for the business case.

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