



**International Global Navigation Satellite Systems Society
IGNSS Symposium 2007**

The University of New South Wales, Sydney, Australia
4 – 6 December, 2007

A real time multi-channel GPS positioning system architecture

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ABSTRACT

The design of a system to deliver GPS observables for tracking multiple remotes in real time is discussed. The key objectives of this architecture are to allow the use of multiple small battery operated rovers and to provide low latency position measurements at a fixed central point. The GPS raw data is transmitted via a telemetry system to the central point, then presented to multiple Kalman filters. The selection of a GPS receiver for the application and design of the system architecture to distribute the load to multiple Kalman filters presents some interesting challenges. The focus of this paper is on the components, the architecture used to deliver the demanding real time processing requirements and the benefits of the system.

KEYWORDS: GPS receiver, Raw Data, DGPS, Telemetry

1. INTRODUCTION

In a conventional Differential GPS (**DGPS**) system the reference station corrections are fed into the GPS receiver where the position solution is to be generated. Processing of both the local and reference station measurements is carried out by the on-board software to deliver a more accurate solution.

When a number of GPS receivers are to be used to track multiple objects in real time, conventional DGPS architecture quickly becomes impractical due to the increase in communications requirements both to and from the receivers. In this case a more efficient architecture is required. By choosing to extract only the raw data (pseudoranges and carrier phase) from each GPS receiver and delivering this via a specially designed telemetry link, the communications requirements are significantly reduced. Using this approach, CPU intensive DGPS processing functions can now be centralised at the telemetry collection point. Additional benefits are gained by reducing the size, weight and power consumption of both the GPS receiver and telemetry transmitter (Rover).

2. SYSTEM ARCHITECTURE

2.1 General

The components used to build this system are mostly from “off-the-shelf” sources where possible to allow the development effort to focus on the design of the unknown pieces of the system. Standard PC's running Windows XP are used to run all software except for the embedded signal processing and software. The aim is to deliver a position solution from each GPS receiver at 10Hz.

2.2 GPS receiver selection

A Thales (formerly Ashtech) G12 is used for the differential reference station function because of its reputation for supplying good code and carrier phase at 10Hz. This is partly due to a superior narrow correlator to help eliminate multi-path signals.

Because of the requirement for pseudorange and carrier phase at a sample rate of 10Hz from the rover, there are fewer suitable GPS receivers and/or receiver chip sets available with this capability. With a view to building an integrated rover, a number of GPS receiver chip sets including SiRF, ST, Conexant and others were examined. All of these have one or more of the key capabilities missing, while some are unsuitable on the basis of power consumption alone.

The Novotel (formerly BAE Systems, formerly CMC) Superstar 2 (**SS2**) was selected as the rover receiver (Novatel Inc. 2005). The SS2 and the Novatel Allstar both use a similar chip set made by Zarlink and share the same triple down conversion design. The main difference between these two receivers is that the Allstar uses the stand alone correlator chip GP2021 (Zarlink Semiconductor 2003), while the SS2 has the ARM CPU integrated into a combined ASIC GP4020 (Zarlink Semiconductor 2002). Both of these receivers supply good code and carrier phase at 10Hz, but the SS2 uses less power at 1W. Although the SS2 can operate from

3.3 volts the Signal to Noise Ratio (**SNR**) performance of the receiver was found to be less than that of the 5 volt version. This is due to the RF front end down-converter (GP2015) using an on chip 3.3 volt regulator for the Voltage Controlled Oscillator (**VCO**) when operating at 5V. This gives better VCO stability and noise performance in the down conversion process.

The Sigtec MG5003 or MG5001 (Sigtec Pty Ltd 2006) receivers both use the same Zarlink chip set as the SS2. Further development to add carrier phase measurement capability using both Sigtec receivers proved that they can also be interchanged with the SS2, giving the same performance.

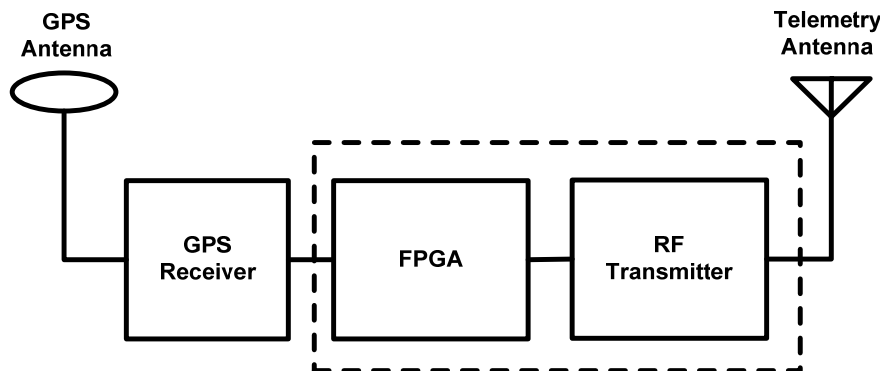
2.3 Rover

The rover consists of three main items: a GPS receiver (as described above), a Field Programmable Gate Array (**FPGA**) and a 2.4GHz transmitter as shown in **Figure 1**.

The FPGA controls both the GPS receiver and the telemetry transmitter. The raw data measurements for all available satellites are extracted by the FPGA then converted into a robust data packet with forward error correction for transmission via the telemetry link. Furthermore, to minimise telemetry bandwidth requirements, the ephemeris data is not included because this information is available from the DGPS reference receiver.

The Cyclone FPGA contains an embedded soft core CPU known as NIOS from Altera (Altera Corporation 2004). Custom designed logic and software are used in the FPGA to meet the accurate synchronising requirements of the system using the 1PPS signal from the GPS receiver. The rover transmits according to a pre-arranged frequency and time sequence.

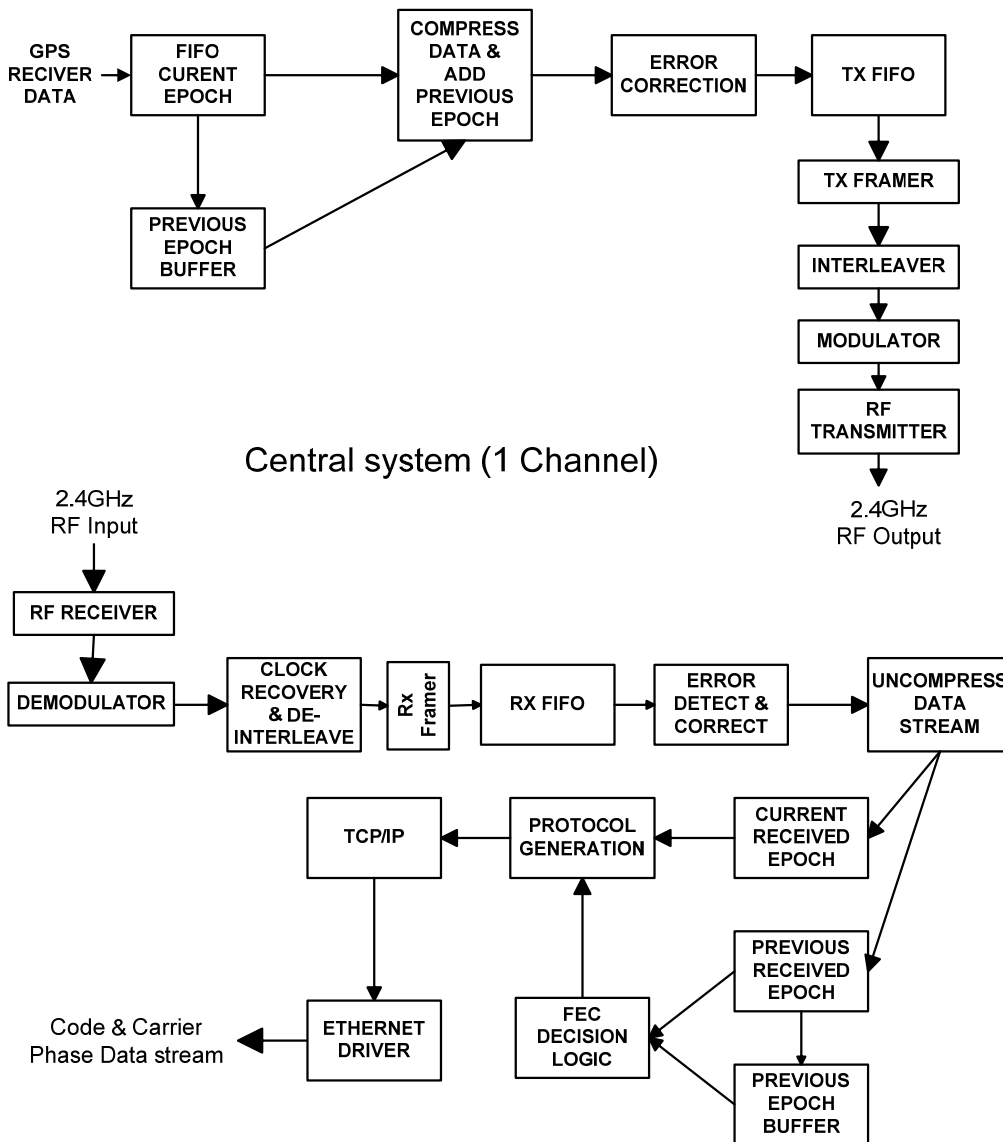
Figure. 1 Rover architecture



2.4 Telemetry system

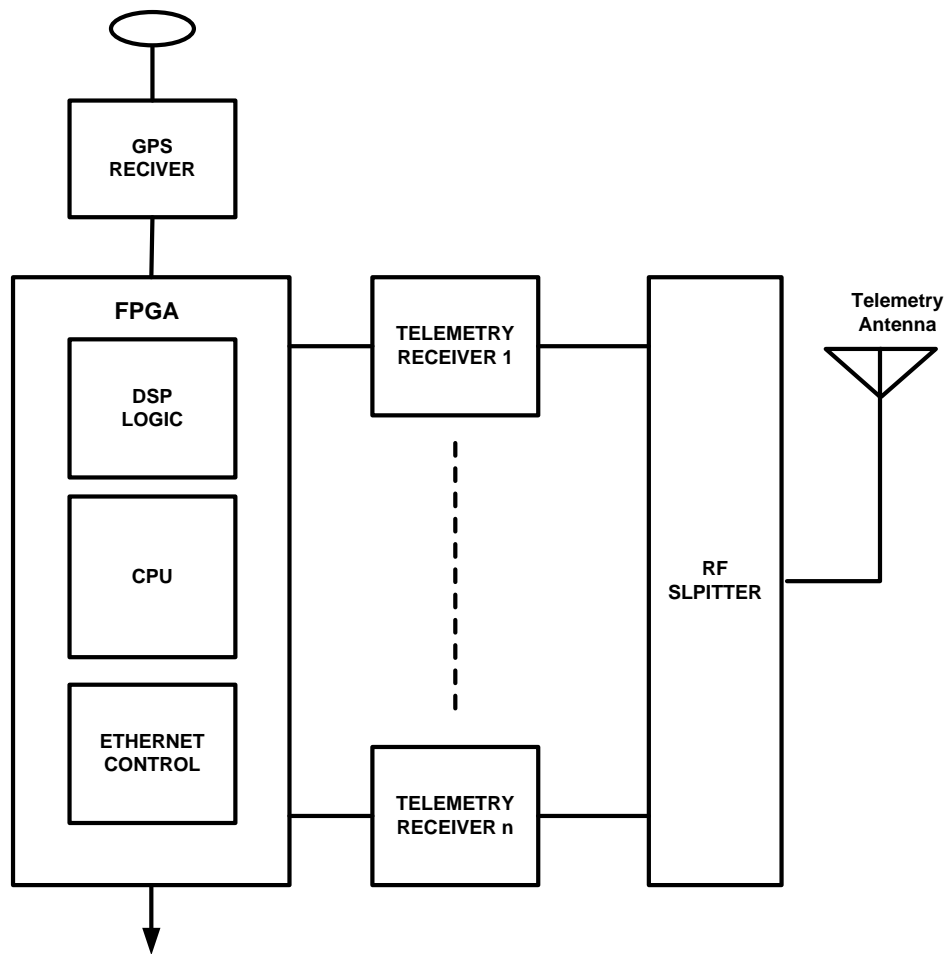
As previously described (Parkinson 2004), the telemetry system uses a combined frequency hopping (**FDMA**) and time synchronised (**TDMA**) scheme to maximise the use of the spectrum. This delivers error corrected raw GPS data packets from multiple rovers to the central point within 100ms. The error correction process uses a convolution encoder at the transmitter and a Viterbi decoder (Viterbi and omura 1979) at the receiving end. A 32 bit Cyclic Redundancy Check code is added to end of the data packet to allow integrity checking of the overall transmission after error correction. See **Figure 2**.

Figure 2. Telemetry data flow



The 2.4GHz ISM band is used with careful attention paid to compliance with ETSI and FCC requirements for spectrum occupancy. At the central receiving point, a single antenna feeds the radio signals from all rovers through a splitter into multiple receivers as shown in **Figure 3**. The receivers are controlled by a central FPGA with an embedded NIOS CPU. The frequency and timing of each receiver is synchronised to GPS 1PPS using a pre-arranged sequence to align with the rover expected transmission. All error correction, time synchronisation and TCP/IP communications are handled in the FPGA.

Figure 3. Central telemetry receiving system



2.5 Central processing system

One rover measurement containing the raw data from all observed satellites is available from the telemetry system every 100ms. However, not every sample is presented to the Kalman filter. A software selection process is used to remove some measurements based on poor satellite health, bad SNR, cycle slip detection, bad time alignment and poor elevation. This improves filter stability by only presenting the best possible measurements.

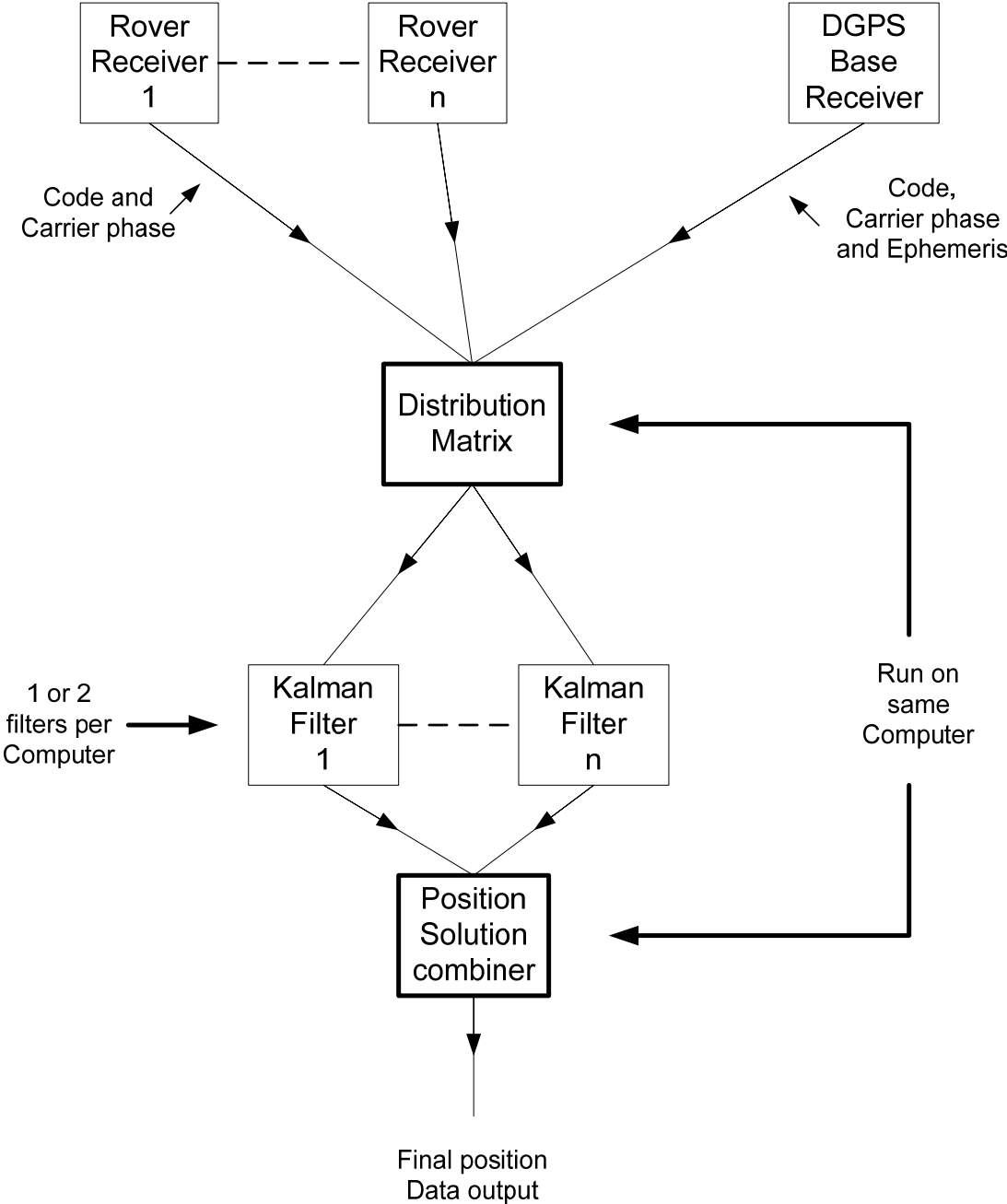
A position solution must be extracted from the filter before the next measurement data is available. This was found to be a significant challenge for a single computer both in terms of both processing power and memory requirement. The problem grows exponentially as the number of rovers increases because the internal matrix requirements of the filter become very large indeed. As suggested (Brown and Hwang 1997), equation (1.1) can be used to estimate the memory requirements for the Kalman filter:

$$M(GB) \approx (r \times 2^{11})^2 \quad (1.1)$$

Where r is the number of rovers and M is the memory size in GB. This estimate predicts that for 32 rovers, the Kalman filter would require over 4Gb of memory, all of which would need to be processed within 100ms.

For this reason, a system was developed to distribute the raw data measurements via a TCP/IP link to a number of separate computers that are dedicated to running the Kalman filters as shown in **Figure 4**. After extracting the solutions from each filter they are re-combined using a software based selection method that accepts or rejects data based on the quality of the solution as reported by the Kalman filter.

Figure 4. Distributed processing



3. CONCLUDING REMARKS

While this architecture is not suitable for small installations of one or two rovers, it remains very scalable to beyond the 30 rovers currently tested.

One possible limitation is the RF spectrum available for use by the telemetry system. The number of possible rovers R_{max} is expressed in equation (1.2) where t_s is the number of TDMA time slots in use.

$$R_{max} = 60t_s \quad (1.2)$$

The current system uses 60 channels in the 2.4GHz ISM spread over 5 time slots per 100ms epoch. Although this suggests a theoretical limit of 300 rovers, because the ISM band is shared with other users, it is unlikely that this maximum can be used when in proximity to other signals.

ACKNOWLEDGEMENTS

This development work was supported by The University of New South Wales, Satellite Navigation & Positioning Laboratory, Sydney and Altera Corporation, USA.

REFERENCES

Altera Corporation (2004). *Altera Cyclone Handbook*.

Brown, R. G. and P. Y. C. Hwang (1997). *Introduction to Random Signals and Applied Kalman Filtering*, John Wiley & Sons.

Novatel Inc. (2005). *Superstar II GPS receiver user manual OM-20000077 Rev 6*.

Parkinson, K. J. (2004). Using GPS to enhance digital radio telemetry. *The 2004 International Symposium on GNSS/GPS*. Sydney.

Sigtec Pty Ltd (2006).

Viterbi, A. and J. K. Omura (1979). *Principles of Digital Communication and Coding*. New York, McGraw-Hill.

Zarlink Semiconductor (2002). GP4020.

Zarlink Semiconductor (2003). GP2021.